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10/613,212	07/07/2003	Youichi Tobita	57454-966	4586

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McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,212	TOBITA, YOUICHI	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/22/06 has been entered.

2. In an amendment dated 4/24/06, the Applicant cancelled claims 10 and 11 and amended claims 1 and 9. Currently claims 1-9 are pending.

Response to Arguments

3. Applicant's arguments, see pages 7 and 8, filed 4/24/06, with respect to the 35 U.S.C. 112 rejection of the limitation "third voltage is substantially at a constant level" have been fully considered and are persuasive. The rejection of the newly added limitation on the merits of enablement has been withdrawn.

4. Applicant's further arguments filed 4/24/06 have been fully considered but they are not persuasive.

On pages 8 and 9 of the Applicant's remarks, the Applicant argues that Shimada does not disclose all of the limitations of claims 1 and 9. Specifically Applicant argues that Shimada does not disclose, "said third voltage is substantially at a constant level." The Applicant cites the different voltages applied during the two different fields as evidence that Shimada's third voltage is not at a constant level.

Examiner respectfully disagrees. The phrases of contention in claims 1 and 9, as currently written, simply require that a substantially constant third voltage be applied during a non-select state to a second gate line, no more. Shimada teaches applying a substantially constant third voltage during an off-period (non-select state) to a second gate line; that Shimada alternates which gate line receives the third voltage every field, does not negate this fact. As such Shimada is seen as sufficiently disclosing all the limitations of claims 1 and 9.

Furthermore the only reason for alternating which gate line receives the third voltage is due to Shimada's assumption that the video signals being applied alternate in polarity (col. 5, lines 29-37). Should this assumption be removed the third voltage would be applied to the same second gate line each off-period.

5. The Applicant's additional arguments stating dependent claims 2-8 are allowable simply due to their inclusion of the limitations of claims 1 and 9 (page 9), are moot in view of Shimada teaching all of the claimed limitations of claim 1.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 5-7, and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (US 5,506,598).

With respect to claim 1, Shimada discloses, a liquid crystal display apparatus comprising: a plurality of pixels arranged in rows and columns, each for providing luminance corresponding to a display voltage; (fig. 2)

a plurality of first gate lines provided corresponding to respective said rows of said plurality of pixels; (G(1,1) and G(2,1) in fig. 2)

a plurality of second gate lines provided corresponding to respective said rows of said plurality of pixels; (G(1,2) and G(2,2) in fig. 2)

a plurality of data lines provided corresponding to respective said columns of said plurality of pixels; (102 in fig. 2)

a gate drive circuit for driving each of said plurality of first and second gate lines to a voltage that is different between a select state in which corresponding one of said rows is selected for a scanning target in accordance with a prescribed scanning cycle and a non-select state except for said select state; (109 in fig. 2)

and a source drive circuit for driving said plurality of data lines to said display voltage that corresponds to the pixels included in the row selected for said scanning target; (108 in fig. 2)

said plurality of pixels each including a liquid crystal element having a pixel electrode and a common electrode for providing luminance that corresponds to a voltage difference between said pixel electrode and said common electrode, (107 in fig. 2)

a first field-effect transistor electrically connected between corresponding one of said data lines and a first node, and having its gate electrically connected to corresponding one of said first gate lines, (103a in fig. 2)

and a second field-effect transistor electrically connected between said first node and said pixel electrode, and having its gate electrically connected to corresponding one of said second gate lines; (103b in fig. 2)

said gate drive circuit setting each voltage of said first and second gate lines in said select state to a first voltage (first field on-period voltage in fig. 7) that can turn-on each of said first and second field-effect transistors, while setting a voltage of said first gate line in said non-select state to a second voltage (G(1,1) first field off-period voltage in fig. 7) that can turn-off said first field-effect transistor as well as setting a voltage of said second gate line in said non-select state to a third voltage (G(1,2) first field off-period voltage in fig. 7, also see col. 3, lines 43-45) that is intermediate between a maximum value and a minimum value of said display voltage (col. 5, lines 53-56; also see the above response to arguments section), *wherein*

said third voltage is substantially at a constant level (Examiner maintains that the first field off-period voltage (G(1,2) in fig. 7) is "substantially at a constant level." It is clear from the figure that the third voltage level is not altered while it is applied to the pixel circuit and thus satisfies the limitations of the claim).

With respect to claim 5, Shimada discloses, the liquid crystal display apparatus according to claim 1 (see above), said gate drive circuit setting said second gate line in the non-select state to said third voltage (G(1,2) first field off-period voltage in fig. 7) in a

normal mode, and setting to a sixth voltage (G(1,2) second field off-period voltage in fig. 7) in a test mode, and a difference between said first and sixth voltages being larger than a difference between said first and third voltages (see fig. 7).

With respect to claim 6, Shimada discloses, the liquid crystal display apparatus according to claim 5 (see above), said sixth voltage (G(1,2) second field off-period voltage in fig. 7) being substantially at a same level as said second voltage (G(1,1) first field off-period voltage in fig. 7).

With respect to claim 7, Shimada discloses, the liquid crystal display apparatus according to claim 1 (see above), said first and second field-effect transistors being formed with an N-type thin film transistor (col. 3, lines 20-23), and said first voltage being higher than said second voltage (see fig. 7).

With respect to claim 9, the limitations of claim 9 are such that claim 9 is rejected on the same merits as those recited in the rejection of claim 1 (see above).

With respect to claim 10, Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada further discloses, that the third voltage (off-period of first field of G(1,2) in fig. 7) is constant among the fields ("Among the fields" is broad terminology. As shown in fig. 7, the third voltage is clearly constant within the first field for transistor G(1,2) and constant once again within the second field for transistor G(1,1). This satisfies the limitation for the third voltage being constant among the fields.).

With respect to claim 11, Shimada discloses the liquid crystal display apparatus according to claim 9 (see above).

Shimada further discloses, that the third voltage (off-period of first field of G(1,2) in fig. 7) is constant among the field ("Among the field" is even broader terminology than that of claim 10. As shown in fig. 7, the third voltage is clearly constant within the first field of G(1,2). This is all that is required to satisfy the limitation that the third voltage be constant among the field.)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Morozumi et al. (US 4,591,848).

With respect to claim 2, Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said common electrode being supplied with a prescribed DC voltage, and said third voltage being substantially at a same level as said prescribed DC voltage.

Morozumi discloses, said common electrode being supplied with a prescribed DC voltage (col. 8, lines 46-47), and said third voltage being substantially at a same level as said prescribed DC voltage (col. 9, lines 32-33, also see fig. 22).

Shimada and Morozumi are analogous art because they are from the same field of endeavor, namely display gate driver circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the common electrode DC voltage as the gate driver voltage, taught by Morozumi, in the drive circuitry of Shimada.

The motivation for doing so would have been to generate a more favorable root-mean-square value of a picture element (Morozumi, col. 9, lines 30-31).

Therefore, it would have been obvious to combine Morozumi with Shimada for the benefit of a more favorable root-mean-square value to obtain the invention as specified in claim 2.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Koden et al. (US 5,465,168).

With respect to claim 3, Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said common electrode being supplied with an AC voltage that is set to one of fourth and fifth voltages in a constant cycle, and said third voltage being substantially at a same level as an average of said fourth and fifth voltage.

Koden discloses, said common electrode being supplied with an AC voltage that is set to one of fourth and fifth voltages in a constant cycle (V1/1 in fig. 12), and said third voltage (0 volts in G1 in fig. 12) being substantially at a same level as an average of said fourth and fifth voltage. (V1/1 average is zero volts).

Shimada and Koden are analogous art because they are from the same field of endeavor, namely display gate driver circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the average of the common electrode AC voltage as the gate driver voltage, taught by Koden, in the drive circuitry of Shimada.

The motivation for doing so would have been to generate a more favorable root-mean-square value of a picture element (Morozumi, col. 9, lines 30-38).

Therefore, it would have been obvious to combine Koden with Shimada for the benefit of a more favorable root-mean-square value to obtain the invention as specified in claim 3.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Yumoto (US 2004/0207615).

With respect to claim 4, Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said gate drive circuit including a plurality of drive units provided corresponding to said rows, respectively; said plurality of drive units each including a first driver for driving corresponding one of said first gate lines with one of said first and second voltages in response to a select signal that indicates whether said corresponding one of said rows s selected for said scanning target, and a second driver for driving corresponding one of said second gate lines with one of said first and third voltages in response to said select signal.

Yumoto discloses, said gate drive circuit including a plurality of drive units provided corresponding to said rows (21 and 23 in fig. 7), respectively; said plurality of drive units each including a first driver for driving corresponding one of said first gate

lines with one of said first and second voltages in response to a select signal (scanB1...scanBN in fig. 7) that indicates whether said corresponding one of said rows selected for said scanning target, and a second driver for driving corresponding one of said second gate lines with one of said first and third voltages in response to said select signal (scanA1...scanAN in fig. 7).

Shimada and Yumoto are analogous art because they are from the same field of endeavor, namely display gate driver circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the gate drive circuitry of Yumoto with the pixel configuration and voltage levels of Shimada.

The motivation for doing so would have been to effectively generate the plurality of voltages that are implemented in Shimada.

Therefore, it would have been obvious to combine Morozumi with Shimada for the benefit of effectively generating voltages to obtain the invention as specified in claim 4.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Kondo et al. (US 6,313,818).

With respect to claim 8, Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said first and second field-effect transistors being formed with a P-type thin film transistor, and said first voltage being lower than said second voltage.

Kondo discloses, said first and second field-effect transistors being formed with a P-type thin film transistor, and said first voltage being lower than said second voltage (col. 2, lines 14-20).

Shimada and Kondo are analogous art because they are from the same field of endeavor, namely active-matrix liquid crystal display devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the N-type transistors of Shimada with the P-type transistors of Kondo.

The motivation for doing so would have been gain the benefit of a smaller subthreshold leakage current.

Therefore, it would have been obvious to combine Kondo with Shimada for the benefit of smaller leakage currents to obtain the invention as specified in claim 8.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

wlb
6/27/06

AMR A. AWAD
PRIMARY EXAMINER